REMARKS

Claims 17-19, 21 and 25-33 are pending in the present application. Replacement claims 17 and 19 have been presented herewith. Also, claims 25-33 have been presented herewith. Claims 1-16, 20 and 22-24 have been canceled. Applicant respectfully reserves the right to file a divisional application including non-elected claims 1-16 and 22-24.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119 and receipt of the certified copy of the priority document.

Drawings

Applicant notes the Examiner's acceptance of the drawings as filed along with the present application on June 19, 2001.

Claim Objections

Claims 17-21 have been objected to because of the informalities listed on page 2 of the current Office Action dated September 30, 2002. The claims have been amended in view of the objections listed by the Examiner. However, claim 19 has not been amended to feature a first resist pattern and a first opening as suggested by the Examiner, because an additional resist pattern and an additional opening are not

featured in claim 19. The Examiner is respectfully requested to withdraw the objection to the claims for at least the above reasons.

Claim Rejections-35 U.S.C. 112

Claims 17-21 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. The claims have been amended in view of the Examiner's suggestions. Applicant respectfully submits that claims 17-19 and 21 are in compliance with 35 U.S.C. 112, second paragraph, and respectfully urges the Examiner to withdraw this rejection for at least the above reasons.

Claim Rejections-35 U.S.C. 103

Claims 17-19 and 21 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Carey et al. reference (U.S. Patent No. 5,075,965), in view of the Pang reference (U.S. Patent No. 6,177,329). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The method of fabricating an IC chip of claim 17 includes in combination "filling the second opening with a metal layer made of an electric connection material", and "etching and removing the third insulating layer and the second insulating layer after said filling the second opening". Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious these features.

The Examiner has interpreted dielectric material 112 as illustrated in Fig. 2 of the

Pang reference as the second insulating layer of claim 17, and apparently dielectric material 134 as illustrated in Fig. 18 as the third insulating layer. The Examiner has further asserted that the Pang reference discloses "etching and removing the third insulating layer and the second insulating layer" in connection with Fig. 24.

As emphasized previously, in the method of fabricating an IC chip of claim 17, the second opening is filled with a metal layer made of an electric connection material, **and thereafter** the third insulating layer and the second insulating layer are etched and removed. However, as described beginning in column 11, line 19 of the Pang reference with respect to Fig. 23, an etching agent is selected to etch both the silicon oxide of dielectric materials 134 and 142, and the silicon nitride of etch stop layer 138. The resultant structure is shown as illustrated in Fig. 24 with photo resist layer 154 removed, and as including narrow air gaps 158 in interconnect layer 152.

Contrary to the Examiner's assertion, the description of the process in connection with Fig. 24 (and also Fig. 23) of the Pang reference does not disclose etching and removing a third insulating layer and a second insulating layer. Particularly, dielectric layers 134 and 112, respectively interpreted by the Examiner as the third and second insulating layers of claim 17, **are not both etched in connection with the description of Figs. 23 and 24 of the Pang reference**. Particularly, dielectric layers 134 and 112 of the Pang reference are not both etched and removed after a second opening is filled with metal layer 150 (interpreted by the Examiner as the metal layer of claim 19). Accordingly, Applicant respectfully submits that the method of fabricating an

IC chip of claim 17 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 17 and 18, is improper for at least these reasons.

Claim 20 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Carey et al. reference in view of the Pang reference, in further view of the Stevens reference (U.S. Patent No. 6,376,374). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

Claim 19 has been amended to include features somewhat similar to dependent claim 20. The method of fabricating an IC chip of claim 19 includes in combination "second etching and removing of the second insulating layer, thereby exposing a top and sidewalls of the conductive material layer", and "dipping a tip end of the exposed conductive material layer including the top and sidewalls thereof into a liquid bath filled with a molten electric connection material". Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious these features.

The Examiner has interpreted conductive material 122 as filled in the corresponding openings illustrated in Fig. 7 of the Pang reference as the conductive material layer of claim 19. However, even though dielectric layer 124 around conductive material 122 is removed as illustrated in Fig. 11 of the Pang reference, one of ordinary skill would have no motivation to modify the method of the Pang reference to dip the top and sidewalls of conductive material 122 of the Fig. 12 structure in a liquid

bath filled with a molten electric connection material.

Particularly, as described beginning in column 8, line 7 with respect to Fig. 13 of the Pang reference, a second layer of dielectric material 134 is formed on the structure of Fig. 12 to purposely create air pockets. There would thus be no reason to dip the Fig. 12 structure of the Pang reference in a liquid bath, since doing so would destroy the intended purpose of the Pang reference, that is the formation of air gaps. Moreover, even assuming for the sake of argument that motivation existed for dipping the structure of Fig. 19 of the Pang reference in a liquid bath (which motivation does not exist), sidewalls of conductive material 122 (interpreted as the conductive material layer of claim 19) would not be exposed or dipped into a molten liquid, regardless of the teaching provided by the Stevens reference. Accordingly, Applicant respectfully submits that the method of fabricating an IC chip of claim 19 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to pending claims 19 and 21, is improper for at least these reasons.

Claims 25-33

Applicant respectfully submits that claims 25-33, as respectively dependent upon claims 17 and 19, distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least the reasons as set forth above, and by further reason of the features therein.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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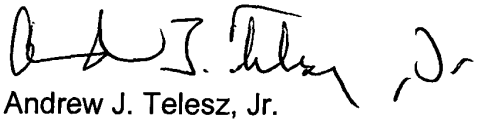

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Enclosures: Version with Marked-Up Changes

VERSION WITH MARKED-UP CHANGES

Additions/Deletions to the Specification:

Page 29, lines 14-20:

An electrode pad 14, a first insulating layer 12, a first photosensitive material layer [62] 60, and a seal member layer 64A are formed on an IC chip 10 shown in FIG. 24A in the same manner as the IC chip 10 of the first embodiment of the invention (See FIG. 1E). Then, as shown in FIG. 24B, the [first] second photosensitive material layer 62 is formed and an opening including the seal member layer 64A is formed in the [first] second photosensitive material layer 62 and the opening is stretched in a horizontal direction.

Page 29, lines 21-25:

As shown in FIG. 24C, a sealing material layer 64B is filled in the opening 20. Likewise, as shown in FIG. 24D, a third photosensitive material layer 66 is formed, then an opening is defined. The opening is formed in a position extended in the [horizontal] vertical direction of the opening as shown in FIG. 24D. The sealing member layer 64C is filled in the opening.

Page 33, lines 11-16:

As shown in FIG. 27C [27A] and FIG. 27D [27B], an insulating layer 85 is formed on a first temporary board 84A by a CVD or [spattering] sputtering technique. Although

it is preferable that the first temporary board 84A is formed of a silicon semiconductor board, [but] it may be formed of other boards such as quartz board and the like. A thickness of insulating layer 85 is preferable to range from 0.5 μm to 1.5 μm.

Page 33, lines 20-26:

Further as shown in FIG. 27D, a groove is formed on the first temporary board 84A while the insulating layer 85 serves as a mask. Thereafter as shown in FIG. 27E, a conductive material layer 88 is deposited on the first temporary board 84A by a [spattering] sputtering technique and the like, then as shown in FIG. 27F, the surface of the first temporary board 84A is polished by a [CHIP] CMP technique and the like. In such a manner, the conductive material layer 88 is embedded in the opening 87.

Additions/Deletions to the Claims:

17. (Amended) A method of fabricating an IC chip comprising [the steps of]:

laminating a first insulating layer on a board;

forming an electrode pad on the board, the electrode pad serving as an input/output terminal;

laminating a second insulating layer over the board and the electrode pad;

forming a first resist pattern on the second insulating layer at a region other than [excepting] a part of the electrode pad;

etching and removing the second insulating layer using [while] the first resist pattern [serves] as a mask, thereby defining [an] a first opening in the second insulating

layer on the electrode pad;

filling the first opening with a conductive material layer made of a conductive material;

laminating a third insulating layer over the second insulating layer and the conductive material layer;

forming a second resist pattern on the third insulating layer at a region other than [excepting] a region of the conductive material layer;

etching and removing the third insulating layer using [while] the second resist pattern [serves] as a mask, thereby defining [an] a second opening in the third insulating layer at the region of the conductive material layer;

filling the second opening with a metal layer made of an electric connection material; and

etching and removing the third insulating layer and the second insulating layer after said filling the second opening.

19. (Amended) A method of fabricating an IC chip comprising [the steps of]:

laminating a first insulating layer on a board;

forming an electrode pad on the board, the electrode pad serving as an input/output terminal;

laminating a second insulating layer over the board and the electrode pad;

forming a resist pattern on the second insulating layer at a region [excepting] other than a part of the electrode pad;

first etching and removing of the second insulating layer using [while] the resist pattern [serves] as a mask, thereby defining an opening in the second insulating layer on the electrode pad;

filling the opening with a conductive material layer made of a conductive material; [and]

second etching and removing of the second insulating layer, thereby exposing a top and sidewalls of the conductive material layer; and

dipping a tip end of the exposed conductive material layer including the top and sidewalls thereof into a liquid bath filled with a molten electric connection material.